SDNAND Memory™
Product specification

Version：V1.0.4

November, 20, 2017

Table of Contents

Change History

Version	Date	Description
V1.0.2	20/11/2016	New Release

A. Product Outline

SDNAND memory is an embedded storage basing on NAND Flash and SD controller. This product has many advantages comparing to raw NAND, it has embedded bad block management, and stronger embedded ECC. Even on abnormal power down it still keep all data safely.

The capacity of SDNAND memory is from 1Gb to 4Gb, and the size is size (8mm x 6mm x0.75mm). The package form is LGA-8.

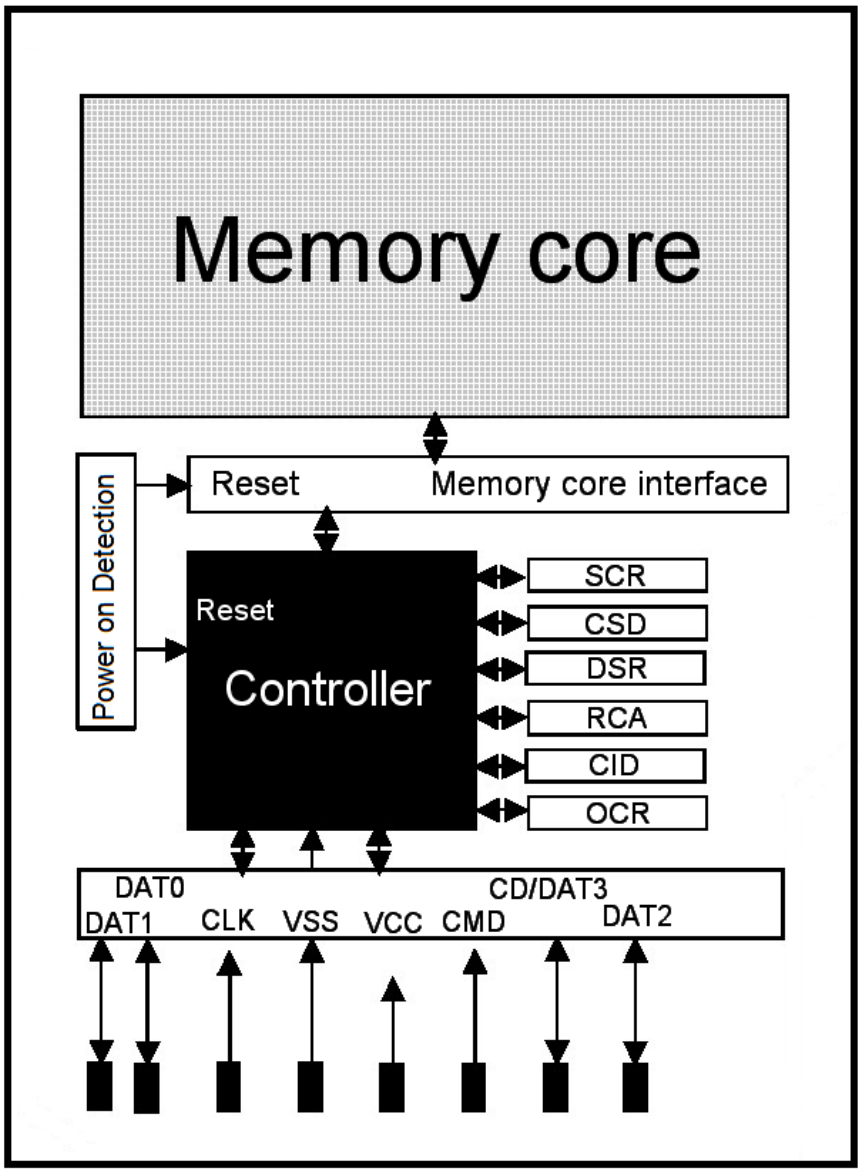
B. Product List

Part No.	Capacity	package	Size	availability
CSNP1GCR01	1Gb	LGA-8	6x8mm	Now
CSNP4GCR01	4Gb	LGA-8	6x8mm	Now
CSNP32GCR01	32Gb	LGA-8	6x9mm	TBD

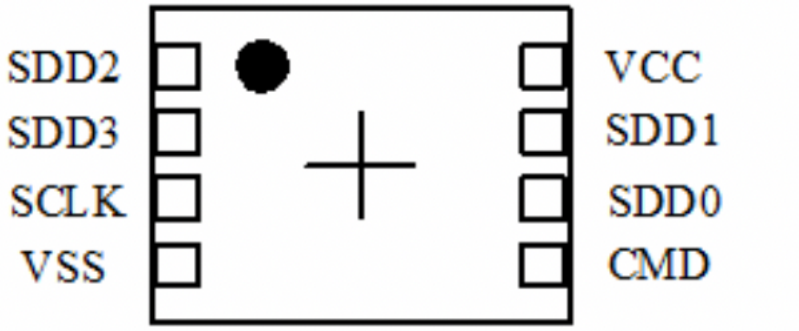
C. Features

- Support Capacity：1Gb-4Gb.
- Support SD system specification version 1.1/2.0.
- Support 1/4 bit mode
- Correction of memory field errors.
- Low power consumption，With the standby energy saving management mode automatically.
- High Speed model，Support Speed class4
- Copyrights Protection Mechanism—Complies with highest security of SDMI standard.
- Operation Temperature：0℃ To 70℃.
- High-speed Flash Controller inside.

D. Block Diagram



E. Pin Assignments(Top View)



PIN #	SD MODE		
	NAME	TYPE[1]	DESCRIPTION
1	DAT2	I/O/PP	Data Line[Bit2]
2	CD/DAT3[2]	I/O/PP[3]	Card Detect/ Data Line[Bit3]
3	SCLK	I	Clock
4	VSS	S	Supply Voltage Ground
5	CMD	PP	Command/Response
6	DAT0	I/O/PP	Data Line[Bit0]
7	DAT1	I/O/PP	Data Line[Bit1]
8	VCC	S	Supply Voltage

Table : SD NAND Contact Pad Assignment

1) S: power supply; I: input; O: output using push-pull drivers; PP: I/O using push-pull drivers ;
2) The extended DAT lines (DAT1-DAT3) are input on power up. They start to operate as DAT lines after SET_BUS_WIDTH command. The Host shall keep its own DAT1-DAT3 lines in input mode, as well, while they are not used. It is defined so, in order to keep compatibility to MultiMediaCards.
3) After power up this line is input with 50KOhm pull-up (can be used for card detection or SPI mode selection). The pull-up should be disconnected by the user, during regular data transfer, with SET_CLR_CARD_DETECT (ACMD42) command

F. Product characteristics

F-1.

Parameter	Range				
	1Gb	4Gb		…	…
Capacity	120MB	481MB		…	…
Write Speed(max)	4MB/S	6MB/s		…	…
Read Speed(max)	15MB/S	15MB/s		…	…
Standby current	150 uA	60uA		…	…
Work current(max)	30mA	55mA		…	…
MTBF	1,000,000 hours				

F-2.

parameter	Range	
Temperature	Work Model	0 ~ 70℃
	Storage Model	- 40 ~ 85℃
Humidity	WorkModel	8% to 95%, Non-condensing
	Storage Model	8% to 95%, Non-condensing

G: Physicial Specifications(unit:mm)

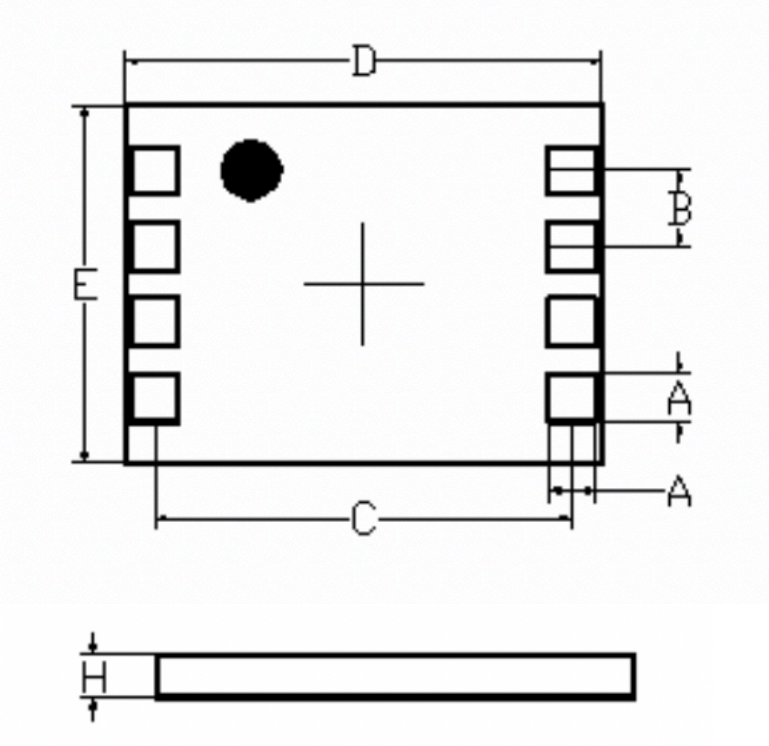


Figure F-1:Mechanical Description

	Common Dimensions			
Symbol	Min	Nom	Max	Note
A	0.65	0.75	0.85	
B	1.17	1.27	1.37	
C	6.90	7	7.10	
D	7.90	8	8.10	
E	5.90	6	6.10	
F	10.90	11	11.1	
H	0.75	0.85	0.95	

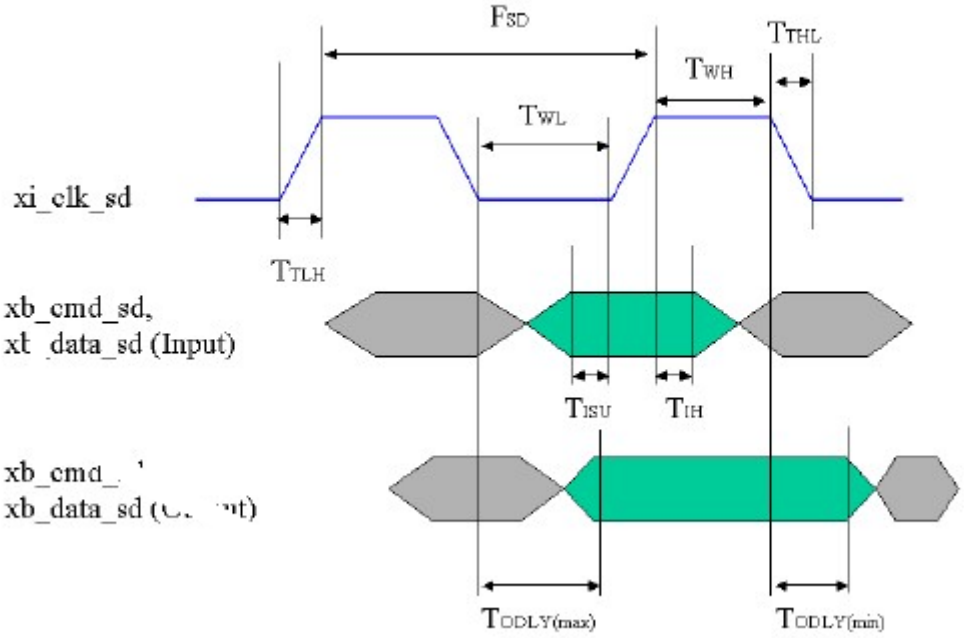
Table: SDNAND Packge Dimensions

H. DC Characteristics

Symbol	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{IL}	Input low voltage		VSS-0.3		0.25VCC	V
V_{IH}	Input high voltage		0.625VCC		VCC+0.3	V
V_{OL}	Output low voltage	IOL=100μA @VCC_min			0.125VCC	V
V_{OH}	Output high voltage	IOH=100μA @VCC_min	0.75VCC			V
I_{IN}	Input leakage current	VIN=VCC or 0	-10	+/-1	10	μA
I_{OUT}	Tri-state output leakage current		-10	+/-1	10	μA
I_{STBY}	Standby current	3.3V@clock stop		0.15	0.18	mA
I_{OP}	Operation current	3.3v@25MHz (Write)		23	25	mA
		3.3v@25MHz (Read)		23	25	mA

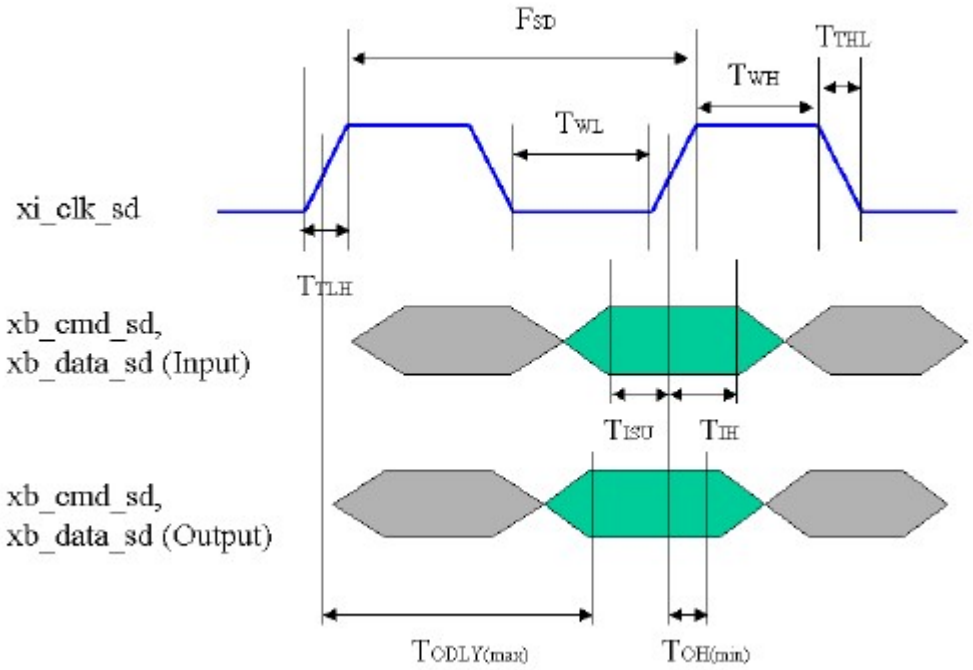
I. AC Characteristics

G-1 Bus Timing(Default Mode)



SYMBOL	PARAMETER	MIN	MAX	UNIT	NOTE
FSD	SD clock frequency	0	25	MHz	
tWL	Clock low time	10		ns	
tWH	Clock high time	10		ns	
tTLH	Clock rise time		10	ns	
tTHL	Clock fall time		10	ns	
tISU	Input setup time	5		ns	
tIH	Input hold time	5		ns	
tODLY	Output delay time	0	14	ns	

G-2 Bus Timing(High-speed Mode)



SYMBOL	PARAMETER	MIN	MAX	UNIT	NOTE
F_{SD}	SD clock frequency	0	25	MHz	
t_{WL}	Clock low time	10		ns	
t_{WH}	Clock high time	10		ns	
t_{TLH}	Clock rise time		10	ns	
t_{THL}	Clock fall time		10	ns	
t_{ISU}	Input setup time	5		ns	
t_{IH}	Input hold time	5		ns	
t_{ODLY}	Output delay time	0	14	ns	
t_{oH}	Output hold time	2.5		ns	

J. Reference Design